ABSTRACT OF THE DISCLOSURE

Each binary carry logic circuit 20 of half adder circuits other than that for the least significant digit comprises a transfer gate 212 turned on when an input bit A2 is active and receiving a carry-in bit *C2 at its data input, and a transistor 23, turned on when the input bit A2 is inactive, connected between a power supply potential VDD and the data output of the transfer gate 212 a signal on which is a carry-out bit *C3. Transfer gates 212 to 214 of binary carry logic circuits other than that for the least significant digit are connected in chain, and are simultaneously on/off controlled by input bits A2 to A4, letting the carry-in bit *C2 from the least significant digit propagate through the transfer gate chain at a high speed.